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1. A method comprising:

maintaining a value for a first counter;

maintaining a value for a second counter based on a content of a non-volatile memory; and

controlling updates to the value for the first counter and to the value for the second counter.

2. The method of claim 1, wherein the controlling comprises updating the value for the second counter when the value for the first counter meets a predetermined condition.

3. The method of claim 1, comprising reading the value for the first counter and the value for the second counter;

wherein the controlling comprises updating the value for the first counter in response to the reading of the value for the first counter and the value for the second counter.

4. The method of claim 1, wherein the controlling comprises updating the value for the second counter upon a power on reset.

5. The method of claim 1, wherein the controlling comprises updating the value for the second counter by a number by programming that number of bit location(s) in a flash memory.

Sub B1 6. The method of claim 1, wherein the controlling comprises updating the value for the second counter by updating a first block of flash memory and updating a second block of flash memory when the first block of flash memory meets a predetermined condition.

7. A method comprising:

reading a value for a monotonic counter, the monotonic counter at least partially basing the value on a content of a non-volatile memory; and

updating the value for the monotonic counter by a number in response to the reading of the value for the monotonic counter.

8. The method of claim 7, wherein the updating the value for the monotonic counter comprises updating a flash memory.

9. A method comprising:

powering on a monotonic counter, the monotonic counter at least partially basing a value on a content of a non-volatile memory; and

updating the value for the monotonic counter by a number in response to the powering on of the monotonic counter.

10. The method of claim 9, wherein the updating the value for the monotonic counter comprises updating a flash memory.

11. An apparatus comprising:

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a first counter to maintain a first value;

a second counter to maintain a second value based on a content of a non-volatile memory; and

control logic to control updating the first and second values.

12. The apparatus of claim 11, wherein the control logic controls the first counter to update the first value when the first and second values are read.

13. The apparatus of claim 11, wherein the control logic controls the second counter to update the second value when the first counter meets a predetermined condition.

14. The apparatus of claim 11, wherein the control logic controls the second counter to update the second value upon a power on reset.

15. The apparatus of claim 11, wherein the non-volatile memory comprises flash memory; and

wherein the control logic controls programming a number of bit location(s) in the flash memory to update the second value.

16. The apparatus of claim 11, wherein the non-volatile memory comprises a first block of flash memory and a second block of flash memory; and

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wherein the control logic controls updating the first block of flash memory and updating the second block of flash memory when the first block of flash memory meets a predetermined condition.

17. An apparatus comprising:

non-volatile memory; and

circuitry to maintain a value for a monotonic counter, the circuitry to base the value at least partially on a content of the non-volatile memory and to update the value by a number in response to a read of the value for the monotonic counter.

18. The apparatus of claim 17, wherein the non-volatile memory comprises flash memory; and

wherein the circuitry updates the value by the number by programming that number of bit location(s) in the flash memory.

19. The apparatus of claim 17, wherein the non-volatile memory comprises a first block of flash memory and a second block of flash memory; and

wherein the circuitry updates the first block of flash memory by the number and updates the second block of flash memory if the first block of flash memory meets a predetermined condition.

20. An apparatus comprising:

non-volatile memory; and

Sub B1 circuitry to maintain a value for a monotonic counter, the circuitry to base the value at least partially on a content of the non-volatile memory and to update the value by a number in response to a powering on of the circuitry.

21. The apparatus of claim 20, wherein the non-volatile memory comprises flash memory; and

wherein the circuitry updates the value by the number by programming that number of bit location(s) in the flash memory.

22. The apparatus of claim 20, wherein the non-volatile memory comprises a first block of flash memory and a second block of flash memory; and

wherein the circuitry updates the first block of flash memory by the number and updates the second block of flash memory if the first block of flash memory meets a predetermined condition.

23. An apparatus comprising:

one or more registers to store a first value;

a first adder to maintain the first value;

flash memory;

one or more registers to store a second value;

a second adder to maintain the second value based on one or more programmed bit locations in the flash memory; and

a control engine to control the flash memory and the first and second adders.

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24. An apparatus comprising:

flash memory;

one or more registers to store a value;

an adder to maintain the value based on one or more programmed bit locations in the flash memory; and

a control engine to control the flash memory and the adder to update the value by a number in response to a read of the value.

25. An apparatus comprising:

flash memory;

one or more registers to store a value;

an adder to maintain the value based on one or more programmed bit locations in the flash memory; and

a control engine to control the flash memory and the adder to update the value by a number upon a power on reset.

26. A computer system comprising:

(a) a monotonic counter comprising:

(i) a first counter to maintain a first value,

(ii) a second counter to maintain a second value based on a content of a non-volatile memory, and

(iii) control logic to control updating the first and second values; and

(b) one or more processors to read the first and second values.

27. The computer system of claim 26, wherein the control logic controls the first counter to update the first value when the first and second values are read.

28. The computer system of claim 26, wherein the control logic controls the second counter to update the second value when the first counter meets a predetermined condition.

29. The computer system of claim 26, wherein the control logic controls the second counter to update the second value upon a power on reset of the monotonic counter.

30. A computer readable medium having computer executable instructions for:

maintaining a value for a first counter;

maintaining a value for a second counter based on a content of a non-volatile memory; and

controlling updates to the value for the first counter and to the value for the second counter.